

IN THE CLAIMS

Please amend the claims as follows:

1. Cancel.
2. Cancel.
3. Cancel.
4. Cancel.
5. Cancel.
6. Cancel.
7. Cancel.
8. Cancel.
9. Cancel.
10. Cancel.
11. Cancel.
12. Cancel.
13. Cancel.
14. Cancel.
15. Cancel.
16. Cancel.
17. Cancel.
18. Cancel.
19. Cancel.
20. Cancel.
21. Cancel.
22. Cancel.
23. Cancel.
24. Cancel.
25. Cancel.
26. Cancel.
27. Cancel.
28. Cancel.
29. Cancel.

Appl. No. 10/066,115
Amdt. dated 9/7/06
Reply to Office Action of 5/12/06

PATENT
Docket: 020103

- 30. Cancel.
- 31. Cancel.
- 32. Cancel.
- 33. Cancel.
- 34. Cancel.
- 35. Cancel.
- 36. Cancel.
- 37. Cancel.
- 38. Cancel.
- 39. Cancel.
- 40. Cancel.
- 41. Cancel.
- 42. Cancel.
- 43. Cancel.
- 44. Cancel.
- 45. Cancel.
- 46. Cancel.

47. (Currently amended) A circuit including a compensation branch for reducing second order non-linear distortion in a receiver ~~caused by jammers during direct down conversion of a received RF signal by the receiver~~, the compensation branch comprising being adapted to be coupled to the receiver to reproduce the second order nonlinear distortion in the receiver and including:

a squaring circuit for receiving ~~the a~~ received RF signal provided to an input of a mixer in the receiver and generating a squared version of the received RF signal;

a gain stage for receiving the squared version of the received RF signal and ~~generating the reproduced~~ reproducing second order nonlinear distortion in the receiver; and

an output coupling circuit for coupling the reproduced second order nonlinear distortion to an output of the receiver to generate a down-converted baseband signal characterized with reduced second order nonlinear distortion.

48. (Currently amended) The circuit of claim 47, ~~wherein the receiver comprises a mixer, and~~ wherein the output coupling circuit couples the reproduced second order nonlinear distortion to an output of the mixer.

49. (Previously presented) The circuit of claim 47, wherein the receiver is a Zero-IF direct down conversion receiver.

50. (Previously presented) The circuit of claim 47, wherein the receiver is a low IF direct down conversion receiver.

51. (Previously presented) The circuit of claim 47, wherein the output coupling circuit is an adder.

52. (Currently amended) The circuit of claim 47, ~~whereby the receiver includes a mixer,~~ wherein the squaring circuit is part of the mixer, and wherein the gain stage receives the squared version of the received RF signal from the mixer.

53. (Currently amended) The circuit of claim 48, ~~whereby the receiver includes a mixer,~~ wherein the squaring circuit is part of the mixer, and wherein the gain stage receives the squared version of the received RF signal from the mixer.

54. (Currently amended) The circuit of claim 49, ~~whereby the receiver includes a mixer,~~ wherein the squaring circuit is part of the mixer, and wherein the gain stage receives the squared version of the received RF signal from the mixer.

55. (Currently amended) The circuit of claim 50, ~~whereby the receiver includes a mixer,~~ wherein the squaring circuit is part of the mixer, and wherein the gain stage receives the squared version of the received RF signal from the mixer.

56. (Currently amended) The circuit of claim 51, ~~whereby the receiver includes a mixer,~~ wherein the squaring circuit is part of the mixer, and wherein the gain stage receives the squared version of the received RF signal from the mixer.

57. (Previously presented) The circuit of claim 47, wherein the receiver defines a receiver path and the compensation branch operates to provide feed forward second-order non-linear distortion reduction to the receiver path.

58. (Currently amended) The circuit of claim ~~48-52~~, wherein the receiver defines a receiver path and the compensation branch operates to provide feed forward second-order non-linear distortion reduction to the receiver path.

59. (Currently amended) The circuit of claim ~~49-53~~, wherein the receiver defines a receiver path and the compensation branch operates to provide feed forward second-order non-linear distortion reduction to the receiver path.

60. (Currently amended) The circuit of claim ~~57-54~~, whereby the non-linear distortion reduction ~~elimination~~ does not introduce other non-linear distortion in the receiver path.

61. (Currently amended) The circuit of claim ~~50-55~~, wherein the receiver defines a receiver path and the compensation branch operates to provide feed forward second-order non-linear distortion reduction to the receiver path.

62. (Currently amended) The circuit of claim ~~59-55~~, whereby the non-linear distortion ~~reduction elimination~~ does not introduce other non-linear distortion in the receiver path.

63. (Previously presented) The circuit of claim 47, further comprising means for adjusting the gain stage to permit calibration thereof.

64. (Previously presented) The circuit of claim 63, wherein the means for adjusting enables factory calibration of a mobile device including the circuit and the receiver.

65. (Previously presented) The circuit of claim 63, wherein the means for adjusting includes circuitry for providing self-contained auto-calibration.

66. (Previously presented) The circuit of claim 49, further comprising means for adjusting the gain stage to permit calibration thereof.

67. (Previously presented) The circuit of claim 66, wherein the means for adjusting enables factory calibration of a mobile device including the circuit and the receiver.

68. (Previously presented) The circuit of claim 66, wherein the means for adjusting includes circuitry for providing self-contained auto-calibration.

69. (Previously presented) The circuit of claim 50, further comprising means for adjusting the gain stage to permit calibration thereof.

70. (Previously presented) The circuit of claim 69, wherein the means for adjusting enables factory calibration of a mobile device including the circuit and the receiver.

71. (Previously presented) The circuit of claim 69, wherein the means for adjusting includes circuitry for providing self-contained auto-calibration.

72. (Previously presented) The circuit of claim 47, wherein the circuit and receiver are on a single integrated circuit.

73. (Previously presented) The circuit of claim 72, wherein the integrated circuit is adapted to be coupled to a mobile station modem (MSM) for signal processing of the down-converted baseband signal.

74. (Previously presented) The circuit of claim 73, wherein the integrated circuit and MSM are further adapted to be used with a transmitter, the integrated circuit being responsive to a test signal generated under MSM control to provide calibration.

75. (Previously presented) The circuit of claim 49, wherein the circuit and receiver are on a single integrated circuit.

76. (Previously presented) The circuit of claim 75, wherein the integrated circuit is adapted to be coupled to a mobile station modem (MSM) for signal processing of the down-converted baseband signal.

77. (Previously presented) The circuit of claim 76, wherein the integrated circuit and MSM are further adapted to be used with a transmitter, the integrated circuit being responsive to a test signal generated under MSM control to provide calibration.

78. (Previously presented) The circuit of claim 50, wherein the circuit and receiver are on a single integrated circuit.

79. (Previously presented) The circuit of claim 78, wherein the integrated circuit is adapted to be coupled to a mobile station modem (MSM) for signal processing of the down-converted baseband signal.

80. (Previously presented) The circuit of claim 79, wherein the integrated circuit and MSM are further adapted to be used with a transmitter, the integrated circuit being responsive to a test signal generated under MSM control to provide calibration.

81. (Currently amended) An integrated circuit having a receiver and a distortion reduction circuit for reducing second order non-linear distortion in ~~a the receiver caused by jammers during direct down conversion of a received RF signal by the receiver~~, the distortion reduction circuit ~~comprising including a compensation branch coupled to the receiver to reproduce the second order nonlinear distortion in the receiver, the compensation branch including:~~

a squaring circuit for receiving ~~the a~~ received RF signal provided to an input of a mixer in the receiver and generating a squared version of the received RF signal;

a gain stage for receiving the squared version of the received RF signal and ~~generating the reproduced reproducing~~ second order nonlinear distortion in the receiver; and

an output coupling circuit for coupling the reproduced second order nonlinear distortion to an output of the receiver to generate a down-converted baseband signal characterized with reduced second order nonlinear distortion.

82. (Previously presented) The integrated circuit of claim 81, wherein the receiver is one of a Zero-IF and a low IF direct down conversion receiver.

83. (Previously presented) The integrated circuit of claim 82, further including means for adjusting the gain stage to permit calibration thereof.

84. (Currently amended) The integrated circuit of claim 83, wherein the means for adjusting enables factory calibration of a mobile device including the integrated circuit ~~and the receiver~~.

85. (Currently amended) The integrated circuit of claim 83, wherein the means for adjusting includes circuitry for providing self-contained auto-calibration.

86. (Currently amended) A circuit for reducing second order non-linear distortion in a receiver ~~caused by jammers during direct down conversion of a received RF signal by the receiver, the circuit being adapted to be coupled to the receiver in a feed forward manner to remove unwanted second order nonlinear distortion in the receiver~~, the circuit comprising:

a squaring circuit for receiving ~~the~~ a received RF signal provided to an input of a mixer in the receiver and generating a squared version of the received RF signal;

a gain stage for receiving the squared version of the received RF signal and generating ~~the unwanted second order nonlinear distortion in the receiver~~; and

an output coupling circuit for subtracting the unwanted second order nonlinear distortion from an output of the receiver to generate a down-converted baseband signal characterized with reduced second order nonlinear distortion.

87. (Previously presented) The circuit of claim 86, wherein the receiver is one of a Zero-IF and a low IF direct down conversion receiver.

88. (Previously presented) The circuit of claim 87, further comprising means for adjusting the gain stage to permit calibration thereof.

89. (Previously presented) The circuit of claim 88, wherein the means for adjusting enables factory calibration of a mobile device including the circuit and the receiver.

90. (Previously presented) The circuit of claim 88, wherein the means for adjusting includes circuitry for providing self-contained auto-calibration.

91. (Currently amended) ~~In a circuit adapted to be coupled to a receiver in a feed forward manner to remove unwanted second order nonlinear distortion in the receiver caused by jammers, a~~ A method comprising:

generating a squared version of a received RF signal provided to an input of a mixer in a receiver;

reproducing, ~~by the circuit, the~~ unwanted second order nonlinear distortion in the receiver based on the squared version of the received RF signal; and

subtracting, ~~using a feed forward technique,~~ the unwanted second order nonlinear distortion from an output of the receiver to generate a down-converted baseband signal characterized with reduced second order nonlinear distortion.

92. (Currently amended) The method of claim 91, further comprising calibrating ~~the a gain used to reproduce the unwanted second order nonlinear distortion stage.~~

93. (Currently amended) The circuit of claim ~~47-52~~, wherein the squared version of the received RF signal is internally generated by the mixer.

94. (Currently amended) The circuit of claim ~~47-52~~, wherein the mixer comprises cross-coupled transistors, wherein the squared version of the received RF signal is internally generated at emitters of the transistors, and wherein the reproduced second order nonlinear distortion is coupled to collectors of the transistors.

95. (Previously presented) The circuit of claim 47, wherein the gain stage generates the reproduced second order nonlinear distortion with a variable gain.

96. (Previously presented) The circuit of claim 95, wherein the variable gain is temperature dependent.

97. (Previously presented) The circuit of claim 47, wherein the gain stage comprises a digital-to-analog converter (DAC) providing a programmable gain for the reproduced second order nonlinear distortion.